REMARKS

The Office Action of April 13, 2007 has been received and its contents carefully considered.

Claims 1-21 are still pending in the application.

Claims 1, 4-9, 12-17 and 20-21 have been rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over the Applicant's Admitted Prior Art (AAPA) (Fig. 1A) in view of Tomobe *et al.* (U.S. Patent 6,198,334). It is submitted that these claims are patentably distinguishable over the cited reference for at least the following reasons.

Invention Not Obvious Where
Prior Art Elements Solve
Different Problem

In the current rejection, Office Action takes the position that configuring the CMOS inverters of AAPA with the PMOS and NMOS transistors as disclosed by **Tomobe *et al.*** to **improve the noise resistance performance** of the phase interpolation circuit would have been obvious to a person of ordinary skills in the art at the time of the invention.

An improvement in noise resistance has never been an issue in the claims or the specification of the Applicants' invention. **Applicants** have detailed the problem to be solved in the abstract of the application, i.e. **avoiding short circuit current**, and the independent claims 1 and 9 recite that the first controlled switch and the second controlled switch serve to avoid a short-circuit current of the phase-interpolation circuit. As can be read in the abstract, the avoidance of a short circuit current of the phase-interpolation circuit that actually results in linearly distributed multiphase signals, should be totally irrelevant to the improvement of noise resistance.

Lindermann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984) is an example where an invention with a combination of old elements and was regarded as nonobvious since the old elements typically dealt with different problems.

Invention Not Obvious By Merely
Demonstrating Elements Of Invention
Independently Known In Prior Art

To resolve the deficiencies of the AAPA, the Office Action points to Tomobe *et al.* as disclosing, in Figure 1, a detailed configuration of a CMOS inverter circuit comprising (1) an input end [INPUT TERMINAL], (2) a first controlled switch [P1], (3) a CMOS inverter [P2, N2], and (4) a second controlled switch [N1]; wherein all [P1, P2, N1, N2] are connected in series. The Office Action appears to take the position that configuring the CMOS inverters of the AAPA (Figure 1A) with PMOS and NMOS transistors connected in series would results in the present invention.

The mechanism to improve noise-resistant performance taught by Tomobe *et al.* (disregarding the fact that this has never been the purpose of the Applicants' invention) involves **PMOS and NMOS transistors with different switching speeds or timings connected in series with a common input terminal** (see abstract and Figure 1 of Tomobe *et al.*). Independent claims 1, 9, and 17 clearly provide that the first inverter, the first controlled switch, and the second controlled switch are all controlled by a first clock signal. It is therefore assumed that the Office Action refers to the CMOS inverter, the PMOS P1, and the NMOS N1 disclosed in Figure 1 of Tomobe *et al.* as elements corresponding to the first inverter, the first controlled switch, and the second controlled switch respectively. The teachings of Tomobe *et al.* in Figure 1 and Figure 2, if adapted to the invention as

stated in claim 1, would prevent **the first inverter and the first controlled switch** (the first clock signal in a second state) or **the first inverter and the second controlled switch** (the first clock signal in a first state) from turning on or off simultaneously. It should be well known by those with ordinary skills of the art that the teachings of Tomobe *et al.* would only help in the improvement of noise resistance by **preventing instantaneous conduction of electric current** between the first inverter and the first controlled switch (the first clock signal in a second state) or between the first inverter and the second controlled switch (the first clock signal in a first state). The problem of a short circuit current existing in the AAPA (Figure 1A) **flows by way of the first inverter and the second inverter**, where **the second inverter is controlled by a totally different second clock signal**, and is therefore apparent that the invention does not benefit from the teachings of Tomobe *et al.*.

The test for obviousness should not be determined by whether the structure of one reference might be bodily incorporated into another reference. Combined teachings that render the claimed subject matter obvious should be observed instead. Please refer to *In re* Wood, 599 F.2d 1032, 202 USPQ 171, 174 (C.C.P.A. 1979); *In re* Bozek, 416 F.2d 1385, 1390, 163 USPQ 545, 549-50 (C.C.P.A. 1969); *In re* Mapelsden, 329 F.2d 321, 322, 141 USPQ 30, 32 (C.C.P.A. 1964).

Invention Not Obvious When
Either Prior Art Reference Teaches
Away From Combination

It is taught by Tomobe *et al.* (abstract) that **different switching speeds or switching timings** of the MOS transistors connected in series help eliminate noise. However, the different switching speeds or switching timings between the first inverter and

the first controlled switch (the first clock signal in a second state) or between the first inverter and the second controlled switch (the first clock signal in a first state) as recited in independent claims 1, 9, and 17 might **cause malfunction when incorporated with the phase interpolation circuit** revealed in the AAPA. The delay of switching would alter the phase of the first clock signal, resulting in **erroneous phase interpolated results**, and may even **increase the short circuit current**, which worsens the problem of the AAPA. Therefore, this invention should not be held obvious since Tomobe *et al.* teaches away from the combination with the AAPA. Please see *In re* Rudko, Civ. 98-1505 (Fed. Cir. May 14, 1999).

Invention Not Obvious When
Combination Of Prior Art Elements Yield
Unpredictable Results

A reasonable assumption about the combination of AAPA and the Tomobe *et al.* patent would be a phase interpolation circuit generating-noise eliminated multiphase signals. However, the actual outcome of the invention implemented according to claims 1, 9 and 17 is the generation of linearly distributed multiphase signals with a good 50% duty cycle but without apparent noise elimination. By yielding unpredictable results, the combination of Tomobe *et al.* and the AAPA is undoubtedly nonobvious. See KSR Int'l v. Teleflex, Inc., 550 U.S. ___(2007).

Supplementary Arguments
Regarding Previous Response

The Office Action appears to take the position that Applicants' earlier argument regarding an inverter circuit with **only one input terminal for an input signal** of Tomobe

et al. (the input signal corresponding to the first clock signal of claims 1, 9 and 17 of the invention) is an argument against the Tomobe *et al.* patent individually. Applicants respectfully disagree.

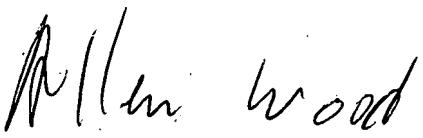
If noise elimination had been a problem addressed by the invention, which actually is not the case, the different switching speeds or switching timings controlled by input signals should be applied in the same fashion, i.e. to have **only one input terminal for the first controlled switch, the first inverter and the second controlled switch** (controlled by the first clock signal of the invention), and to have also **only one input terminal for the first controlled switch, the second inverter and the second controlled switch** (controlled by the second clock signal of the invention) in order to generate a noise-eliminated interpolated output signal. However, referring to Figure 4B, the first controlled switch, the second inverter and the second controlled switch do not share a common input terminal. Therefore, a series that involves the first controlled switch, the second inverter, and the second controlled switch would not benefit from the teachings of the Tomobe *et al.* patent to solve the problem revealed in the AAPA.

For at least the aforementioned reasons, it is respectfully submitted that independent claims 1, 9 and 17, as well as their dependent claims, are distinguishably patentable over the cited references, and the rejection of these claims be withdrawn.

Conclusion

Accordingly, it is submitted that all of the pending claims are allowable over the cited references, so that this application is in condition for allowance. Such action and the passing of this case to issue are therefore respectfully requested.

Respectfully submitted,



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